A Layered Architecture for Quantum Computing Using Quantum Dots

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Abstract. We address the challenge of designing a quantum computer architecture with a layered framework that is modular and facilitates fault-tolerance. The framework is flexible and could be used for analysis and comparison of differing quantum computer designs. Using this framework, we develop a complete, layered architecture for quantum computing with optically controlled quantum dots, showing how a myriad of technologies must operate synchronously to achieve fault-tolerance. Our design deliberately takes advantage of the large possibilities for integration afforded by semiconductor fabrication. Quantum information is stored in the electron spin states of a charged quantum dot controlled by ultrafast optical pulses. Optical control makes this system very fast, scalable to large problem sizes, and extensible to quantum communication or distributed architectures. The design of this quantum computer centers on error correction in the form of a topological surface code, which requires only local and nearest-neighbor gates. We analyze several important issues of the surface code that are relevant to an architecture, such as resource accounting and the use of Pauli frames. Furthermore, we investigate the performance of this system and find that Shor's factoring algorithm for a 2048-bit number can be executed in approximately one week.

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Contents

1. Introduction to the Layered Architecture

A computer architecture defines and organizes the components of a system, their roles, and the interfaces between them. In computer systems, the architecture of a system determines its performance, the difficulty of implementation, and its flexibility. A good architecture exposes the strengths of its underlying technologies while avoiding unnecessary dependence on a specific technology, allowing independent evolution over time, and occasionally wholesale replacement of components or subsystems. Developing a flexible framework is particularly important for the nascent field of quantum computing, where relatively little work on architecture has been performed. This problem is important since an architecture provides structure, not only for the quantum computer itself but also for the designers — organizing the system design can also serve to organize the conceptual and logistical problems of engineering a computer.

Here, we propose a layered architecture for quantum computing which is both *modular* and *fault-tolerant*. The objective is to develop a framework for building up a quantum computer from individual components, while also providing a means to compare different approaches to quantum computing, such as nitrogen-vacancy centers in diamond, quantum dots, trapped ions, or atoms in optical lattices [1]. This architecture has many universal aspects applicable to different physical hardware, but to make this discussion concrete, we introduce a new quantum computer architecture based on **Qu**antum **D**ots with **O**ptically-controlled **S**pins, or QuDOS. The organizing principles of the architecture are explained as this specific quantum computer implementation is developed step-by-step.

1.1. Prior Work on Quantum Computer Architecture

Many different quantum computing technologies are under experimental investigation [1]. Since DiVincenzo introduced his fundamental criteria for a viable quantum computing technology [2] and Steane emphasized the difficulty of designing systems capable of running quantum error correction (QEC) adequately [3,4], several groups of researchers have outlined various additional taxonomies addressing the architectural needs of large-scale systems [5, 6]. For many technologies, small-scale interconnects have been proposed, but the problems of organizing subsystems using these techniques into a complete architecture for a large-scale system have been addressed by only a few researchers. In particular, the issue of heterogeneity in systems has received relatively little attention.

Kielpinski *et al.* proposed a scalable ion trap technology utilizing separate memory and computing areas [7]. Because quantum error correction requires rapid cycling across all physical qubits in the system, this approach is best used as a unit cell replicated across a larger system. Other researchers have proposed homogeneous systems built around this basic concept. One common structure is a recursive H tree, which works well with a small number of layers of a Calderbank-Shor-Steane (CSS) code, targeted explicitly at ion trap systems [8,9]. Oskin *et al.* [10], building on the Kane solid-state NMR technology [11], proposed a loose lattice of sites, explicitly considering the issues of classical control and movement of quantum data in scalable systems, but without a specific plan for QEC. Duan and Monroe proposed the use of photonic qubits to distribute entanglement between ions located in distant traps [12], and such photonic channels could be utilized to realize a modular, scalable distributed quantum computer [13]. Fowler *et al.* [14] investigated a Josephson junction flux qubit architecture considering the extreme difficulties of routing both the quantum couplers and large numbers of classical control lines, producing a structure with support for CSS codes and logical qubits organized in a line. Whitney *et al.* [15, 16] have investigated automated layout and optimization of circuit designs specifically for ion trap architectures, and Isailovic *et al.* [17, 18] have studied interconnection and data throughput issues in similar ion trap systems.

With the recent advances in the operation of the topological codes and its desirable characteristics of a high *practical* threshold and need for only nearest-neighbor interactions, research effort has shifted toward architectures capable of building and maintaining large two- and three-dimensional cluster states [19, 20].

The abstract framework of a quantum multicomputer [21] recognizes that large-scale systems demand heterogeneous interconnects; in most quantum computing technologies, it may not be possible to build monolithic systems that contain, couple, and control billions of physical qubits. This architectural framework was extended in a recent paper designed around nanophotonic coupling of electron spin quantum dots that explicitly uses *multiple* levels of interconnect with varying coupling fidelities (hence, purification requirements), as well as the ability to operate with a very low yield of functional devices [22]. Although that proposed system has many attractive features, concerns about the difficulty of fabricating adequately high quality optical components and the desire to reduce the surface code lattice cycle time led to the architecture proposed in this paper.

1.2. Layered Framework

A good architecture must have a simple structure while also efficiently managing the complex array of resources in a quantum computer. Our architecture consists of five layers, where each layer has a prescribed set of duties to accomplish. The interface between two layers is defined by the services a lower layer provides to the one above it. To execute an operation a layer must issue commands to the layer below and process the results. The utility of this scheme is that the many functions in a quantum computer are organized in a manner that aids understanding for the designer and translates directly into an effective control structure for the device itself. By organizing the architecture in layers, we deliberately create a *modular* design for the quantum computer.

The layered framework can be understood by a control stack which organizes the operations in the architecture. Figure 1 shows an example of the control stack for the quantum dot architecture we propose here, but the particular interfaces between layers will vary according to the physical hardware, quantum error correction, etc. that one chooses to implement. At the top of the control stack is the Application layer, where a quantum algorithm is implemented and results are provided to the user. The bottom Physical layer hosts the raw physical processes underpinning the quantum computer. The layers between (Virtualization, Quantum Error Correction, and Logical) are essential for shaping the faulty quantum processes in the Physical layer into a system of high-accuracy *fault-tolerant* qubits and quantum gates at the Application layer.

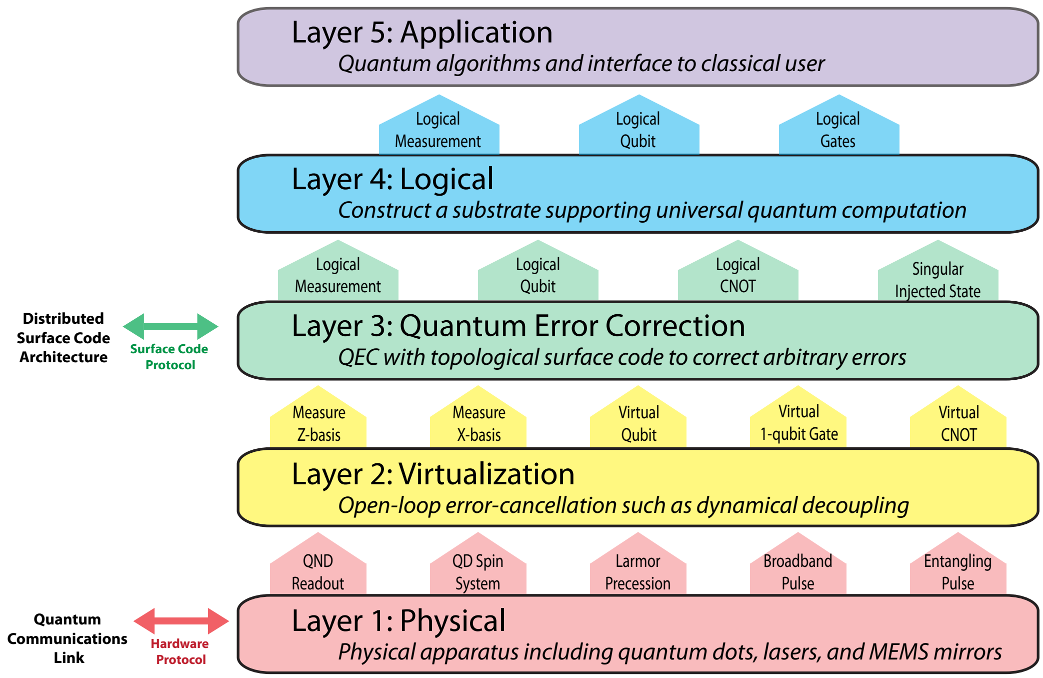

Figure 1. Layered control stack which forms the framework of a quantum computer architecture. Vertical arrows indicate services provided to a higher layer. Arrows on the left margin indicate that communication protocols are necessary to connect multiple quantum information devices, but this topic is outside the scope of this work.

1.3. What is a qubit?

The fundamental unit of information in a quantum computer is the qubit. For our purposes, we reserve the terminology "qubit" for an isolated system where the quantum information is closed under SU(2) algebra [23]. A simple example is a two-level system (TLS), such as the spin of an electron. The reason for this distinction is to reserve "qubit" for its meaning as an information unit, not a physical system. As we will show by example in section 2.1.1, the underlying physical system may be more complex than a TLS, but these details are hidden by layers of abstraction in the architecture. The "qubit" first appears as an output of Layer 2 (Virtualization, section 3), where physical processes are organized into quantum information in the form of "virtual qubits." Layer 3 (Quantum Error Correction, section 4) constructs a "logical qubit" from many virtual qubits and gates. These objects and the processes which create them are explained in detail in subsequent sections.

1.4. Two Ways to Protect Quantum Information

Quantum information is fragile, so the most important role of a fault-tolerant quantum computing architecture is to protect quantum information from errors caused by both coupling to the environment and imperfect control operations. There are two fundamental approaches to protecting qubits used in the layered architecture. The first technique addresses systematic errors, which are correlated in time. When considering decoherence of a qubit, the environment exerts an unknown coupling to the qubit, but perhaps the noise power spectral density of the bath has a characteristic coherence time longer than the timescales of control operations. This situation can be addressed by dynamical decoupling (DD) [24, 25], which is a class of control techniques for reducing qubit decoherence caused by an environment. Similarly, control pulses may have a repeatable bias (such as laser intensity fluctuations), so that the same error is consistent between pulses at different times. Much like DD, there are sequences of pulses known as compensation sequences [26, 27] which reduce control errors by having multiple faulty pulses combine to create a more accurate quantum gate. This collection of techniques resides in Layer 2, the Virtualization layer (see section 3). The purpose of Layer 2 is to take raw physical processes and shape them into the abstract components of quantum information — qubits and quantum gates — which is why the qubit first appears in Layer 2.

The second important method for protecting quantum information is quantum error correction (QEC) [28]. Much like its classical analogue, QEC encodes quantum information in an error-correcting code, which is characterized by the ability to identify and correct arbitrary errors in the fundamental qubits and gates (provided their probability of occurrence is below a certain threshold). The whole of Layer 3 is devoted to QEC, which in this investigation is a topological surface code [29]. In general, other QEC schemes can be incorporated into this architecture. Errors manifest as a "syndrome" found by projective measurement operations in a "syndrome extraction" circuit in the quantum computer. QEC fails when the most likely pattern of errors corresponding to a syndrome is not correct, which happens when error rates are too high (above threshold). The hallmark of QEC is its ability to correct arbitrary errors.

The distinction between Layers 2 and 3 is subtle but important. Qualitatively, it would seem that Layer 2 is open-loop control since the sequence of control operations does not depend on the state of the system, while Layer 3 quantum error correction incorporates feedback by measuring the system and changing future operations conditioned on the measurements. However, the methodology of QEC has advanced so that this is no longer accurate; in particular, the accumulated errors can be handled by Pauli frames (see sections 4.1.2 and 4.2.4). In this manner, "error correction" consists of post-processing measurement results, so feedback into control operations does not occur. Still, while not traditional closed loop control, the quantum measurements do alter the quantum data; in particular they project drifts in the continuous Hilbert space of the virtual qubits into discrete substates which may be analyzed via digital error correction techniques. Another possibility is separating error mitigation techniques by local and non-local control operations. Dynamical decoupling typically uses only local gates, but there is a related concept known as the decoherence-free subspace (DFS) [30] which requires non-local gates (*e.g.* coupling multiple electron spins). A DFS encodes a qubit into a system with many more degrees of freedom; the particular encoding exploits a symmetry in the system so that the subspace spanned by the qubit is invariant to some non-unitary coupling to the environment (decoherence). This behavior is reminiscent of QEC, but there is a crucial distinction that firmly separates DD, DFS, and compensation sequences in Layer 2 from QEC in Layer 3. Layer 2 techniques do not extract information about the state of the quantum computer, whereas Layer 3 does. The information gathered by Layer

3 is not the state of the quantum information being protected, but rather the likely pattern of errors which have occurred. Therefore, Layer 2 does not monitor the state of the system and never uses projective measurement. Layer 3 monitors the system for errors, and accomplishes this with measurement. Nevertheless, Layers 2 and 3 are not redundant; the importance of each, along with their synergy, is discussed in sections 3 and 4.

1.5. Communication Protocols

Just as modern digital computers are frequently networked together, quantum computers may need to share a quantum information connection. To communicate quantum information between two devices, as in quantum repeaters [31] or in a distributed architecture [22], an appropriate communication protocol for Layer 1 (Physical) must be devised. These two quantum computers could be of wholly different technologies (say ion trap vs. quantum dot) if a practicable protocol exists. Moreover, a distributed surface code architecture [22] would also require a communication protocol [32] in Layer 3. The location of these protocols in the layered framework is noted in Figure 1, but this topic is considered outside the scope of the present work.

1.6. Interaction between Layers

For the quantum computer to function efficiently, each layer must issue instructions to layers below in a tightly defined sequence. However, a robust system must also be able to handle errors caused by faulty devices. To satisfy both criteria, a control loop must handle operations at all layers simultaneously while also processing syndrome measurement to correct errors which occur. A prototype for this control loop is shown in Figure 2.

The primary control cycle defines the behavior of the quantum computer in this architecture since all operations must interact with this loop. As discussed later, timing is critically important, so this cycle does not simply issue a single command and wait for the result before proceeding — pipelining is essential [33]. Moreover, Figure 2 describes the control structure needed for the quantum computer. Processors at each layer track the current operation and issue commands to lower layers. Layers 1 to 4 interact in the loop, whereas the Application layer interfaces only with the Logical layer since it is agnostic to the underlying design of the quantum computer.

2. Layer 1: Physical

The physical layer is the foundation of the quantum computer. All truly quantum effects happen here, with higher layers building complicated operations from sequences of processes performed at the physical layer. As a result, the physical layer exists solely to provide services to layers above, and no decision- or branching-based controls run here, as occurs in the upper layers. Implementing a quantum computer architecture begins at Layer 1, where basic hardware for storing and manipulating quantum information is constructed. We illustrate this process with a quantum computer based on the optical control of charged quantum dots known as QuDOS.

2.1. Components of the Physical Layer

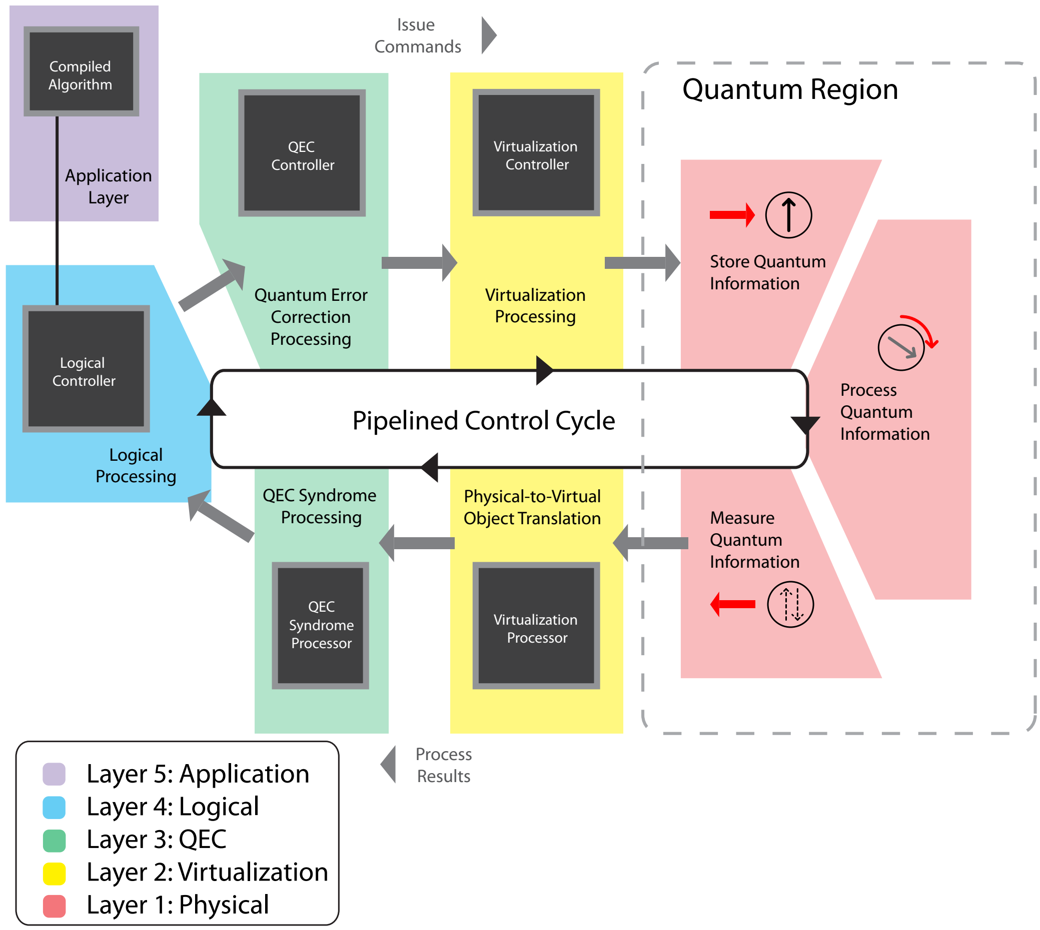

Figure 2. Primary control cycle of the quantum computer. Whereas the control stack in Figure 1 dictates the interfaces between layers, the control cycle determines the timing and sequencing of operations. The dashed box encircling the Physical layer indicates that all quantum processes happen exclusively here, and the layers above process and organize the operations of the Physical layer. The Application layer is external to the loop since it functions without any dependence on the specific quantum computer design.

2.1.1. Electron Spin within a Quantum Dot A quantum computer must have the ability to store information between processing steps. The information carrier in QuDOS is the spin of an electron bound within an InGaAs self-assembled quantum dot (QD) surrounded by GaAs substrate [34–39]. These QDs can be excited to trion states (a bound electron and exciton), which emit light of wavelength $\sim$ 900 nm when they decay. A transverse magnetic field splits the spin levels into two metastable ground states [40], which will later form a two-level system for a virtual qubit in Layer 2. The energy separation of the spin states is important for two reasons related to controlling the electron spin. First, the energy splitting facilitates control with optical pulses as explained in section 2.1.3. Second, there is continuous phase evolution between the two spin states, which in conjunction with optical pulses provides complete unitary control of the electron spin vector.

2.1.2. Planar DBR Microcavity Accessing the quantum properties of a single electron spin system requires an enhanced interaction with light, and so an optical microcavity is necessary. To facilitate the two-dimensional array of the surface code detailed in Layer 3, this microcavity must be planar in design, and so the cavity is constructed from two distributed Bragg reflector (DBR) mirrors stacked vertically with a $\lambda/2$ cavity layer in between. This cavity is grown by molecular beam epitaxy (MBE). The QDs are embedded at the center of this cavity to maximize interaction with antinodes of the cavity field modes. Figure 3 illustrates quantum dots arranged at the center of a planar cavity. Using MBE, high-quality ($Q > 10^5$) microcavities can be grown with alternating layers of GaAs/AlAs [41].

2.1.3. Ultrafast Optical Pulses for Spin-State Rotation The ability to perform fast manipulations of the quantum states stored in a quantum computer is essential for performing operations faster than decoherence processes can corrupt them, as well as for ensuring a fast overall algorithm execution time [6]. In QuDOS, ultrafast optical pulses centered 900–950 nm rotate the spin vector of an electron within a QD [42, 43]. By virtue of being short in duration, these pulses are broad in frequency, facilitating stimulated Raman transitions between the spin levels through excited-state trion levels. Therefore, the complete dynamics of the state rotation depends on a four-level system (consisting of the two metastable spin ground states and two excited trion states). Other control pulses in QuDOS (see sections 2.1.4 and 2.1.6) require a high-Q microcavity which has a narrow transmission window at the cavity resonance; the bandwidth of the broadband pulses is significantly larger than the transmission bandwidth of the cavity resonance. As a result, the broadband pulse cannot be sent directly into the microcavity. This problem is circumvented by sending the broadband pulses at angled (rather than normal) incidence. The cavity response is shifted to higher frequencies, so that a red-detuned pulse can enter the cavity at the first minimum in the cavity reflectivity as a function of frequency. Alternatively, one could send red-detuned pulses at normal incidence, sacrificing the majority of each pulse which is reflected; this approach is only viable if significantly more optical power is available. Figure 3 shows the three laser pulses used in QuDOS, as well as their power spectrums.

2.1.4. Spin Entangling Operation The construction of a practical, scalable two-qubit gate in a quantum dot architecture remains the most challenging element of the hardware. In quantum dots with transverse confinement provided by electrostatic gates, electronic manipulation of the electron wavefunction allows control over the exchange interaction, providing fast ($\sim$ 100 ps) quantum gates, as proposed some time ago [45] and demonstrated in numerous experiments [46]. Employing such gates for a hybrid system with both optical and electrical control is certainly possible, but requires further development of the optical control of electrically defined quantum dots [47]. Entanglement of directly tunnel-coupled vertically stacked InAs quantum dots has also been demonstrated [48], but the scalability of this coupling mechanism

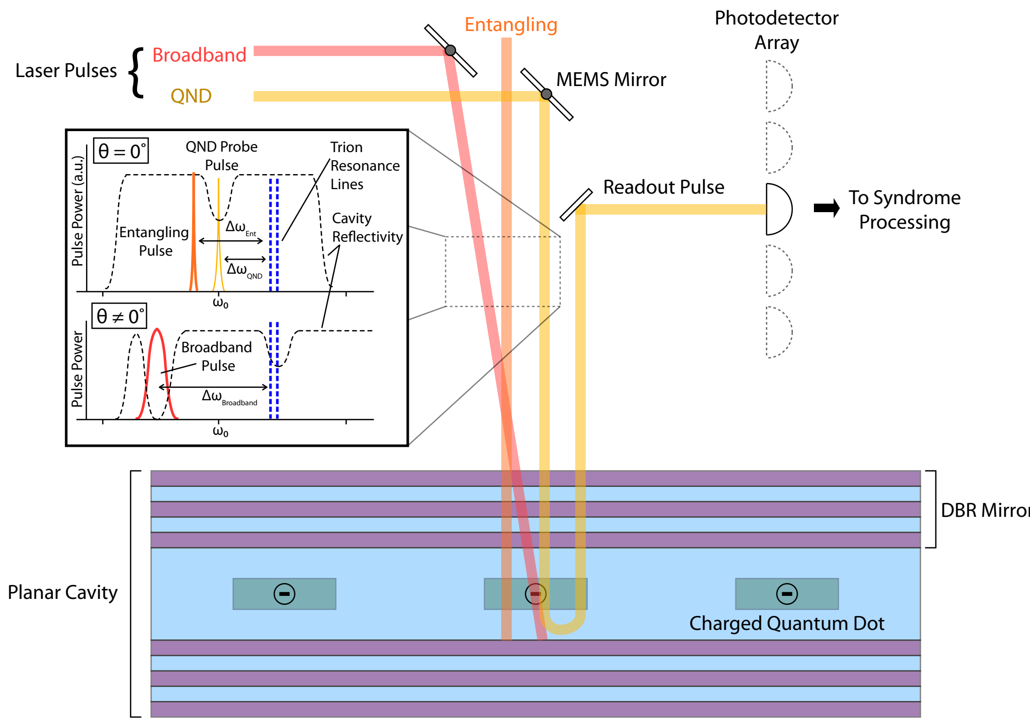

Figure 3. Schematic diagram showing the primary components of the Physical Layer. The inset image shows the spectrum for the various laser pulses that implement different quantum operations. The quantum non-demolition (QND) measurement and entangling pulses are modulated continuous-wave laser pulses, which are narrow in frequency bandwidth; these pulses are sent at normal incidence. The broadband pulses which rotate the electron spin state are angled relative to normal incidence, which shifts the cavity reflectivity response to higher frequencies. This enables the red-detuned pulse to enter the cavity at the first dip in the reflectivity. Each of the different laser pulses has a detuning relative to the trion (excited state) resonance frequency. The entangling pulse is also detuned from cavity resonance in a manner prescribed in Ref. [44].

is uncertain. An exotic but promising possibility includes optically inducing longer-range, exciton-mediated exchange interactions [49, 50].

A fast, all-optically controlled two-qubit gate would certainly be attractive, and early proposals [51] identified the importance of employing the nonlinearities of cavity QED. Ref. [51] suggests the application of two lasers for both single-qubit and two-qubit control; more recent developments have indicated that both single-qubit gates [42, 52] and two-qubit gates [44] can be accomplished using only a single optical pulse. However, the demands on the optical microcavity system are challenging. The critical figure of merit for the cavity QED system is the cooperativity factor C, which is proportional to the cavity quality factor Q divided by the cavity volume V. Large values of this can be achieved via cavities with strong transverse confinement, such as the microdisk cavities proposed in Ref. [51]. This arrangement poses challenges for scalability. An obvious modification is to couple these cavities with waveguides; an architecture employing this approach was discussed in Ref. [22], and in this case substantial additional physical resources are needed to mitigate optical losses at the cavity-waveguide interfaces. For the present architecture, we envision transverse cavity confinement entirely due to the extended microplanar microcavity arrangement, in which cooperativity factors are enhanced by the angle-dependence of the cavity response, an effect which is enlarged by high index of refraction contrast in the alternating mirrors of the DBR stack [34]. While existing cooperativity factors achieved this way are not estimated to be high enough to produce quantum gates which meet the fault-tolerant threshold alone, advanced control techniques and multi-spin encodings (such as for "virtual qubits"; see sections 3.1.1 and 3.2.1) may enable this technology to function with acceptable error rates.

Whether a microplanar microcavity arrangement will offer sufficient nonlinearity for an all-optically controlled dot architecture or whether electronically controlled gates will be employed will depend on forthcoming experimental developments. However, for the purposes of the present architecture, both gates are short range, a constraint handled by the surface code quantum error correction we employ (see section 4) which demands only nearest-neighbor interactions. Short range gates can severely limit the efficacy of other quantum error correction schemes [53]. Long range couplings, for example to form bridges over optically inactive regions of a single chip or for chip-to-chip connections, will likely employ a variety of different quantum optical techniques which sacrifice speed for tolerance to optical loss; for a discussion, see Refs. [22] and [54]. Incorporating such long-distance links into the present architecture must occur at both the Physical and QEC layers; the inclusion of such interconnections into QuDOS is the subject of future work.

2.1.5. Optical Patterns for Control Pulses Parallelism in operations is essential for QuDOS to function efficiently. The quantum operations are driven by laser pulses sent into the planar microcavity (see Figure 3). However, one cannot use a single laser for each quantum dot since such a system would not feasibly scale to a fault-tolerant quantum computer. Instead, this architecture uses a finite set of lasers; each laser can illuminate the entire array of quantum dots, which in QuDOS is estimated to be about 10^9 QDs in size (see section 5.2). To implement desired gates, one must allow this laser light to reach the target quantum dots, while blocking it from interacting with the other QDs. Since the QDs are arranged in a square lattice, one can think of the presence or absence of a light pulse at each as a pixel in an image, and the overall image forms an optical pattern across the surface of the planar cavity. The problem of multiplexing control signals to individual QDs is therefore solved by controlling an optical pattern which illuminates the QD array. Two major challenges must be addressed: (1) the architecture demands control over very many QDs, and (2) the spacing of the QDs is approximately 1 μm apart, which approaches the diffraction limit of the light for control operations ($\sim$ 900 nm). The following sections address each of these concerns individually.

MEMS Micromirrors Optical control of the QD array requires more than simply generating the light pulses with lasers. These pulses must interact with the correct target quantum dots in time and location. We estimate the number of virtual qubits (and hence QDs) needed in this architecture to be on the order of 10^9 (see section

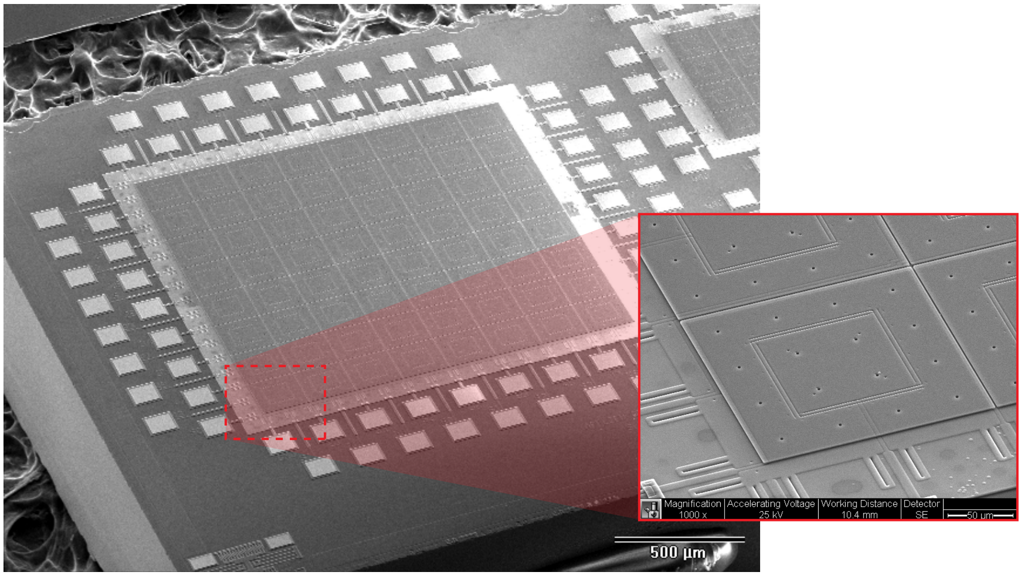

Figure 4. SEM image of an array of micromirrors. This image is an experimental sample of vertically actuated mirrors, whereas the MEMS array in QuDOS would require smaller size mirrors with tilting actuation at very high speeds. The inset image shows a magnified view of a single mirror.

5.2). Multiplexing a single laser to millions of targets is a daunting task, especially integrated into a single system. To achieve this, MEMS micromirrors are fabricated in a two-dimensional array so that each mirror serves as an optical modulator for its corresponding QD [55, 56]. Figure 4 shows an example of 8×8 array of micromirrors fabricated on a silicon substrate, where each mirror acting as a pixel can move vertically to induce piston motion. A much larger array ($\sim 10^6$ pixels) of tilting micromirrors is commercially available for use in projection displays today [57]. The commercial digital mirror devices (DMD) feature a switching time of ~ 5 μs with individual pixel size as small as ~ 10 μm [58]. With further device optimization, a switching time of ≤ 1 μs is feasible [59]. Using this technology, the laser light falling on each pixel can be turned "on" or "off" by reflecting the light towards or away from the QD. The light pattern pointed towards the QD can be imaged onto the QD array using imaging optics and phase-shift masking.

Phase-shift Masking Controlling the individual quantum dots in this computer requires focusing light in a complex pattern with a resolution close to the diffraction limit of the light being used. The quantum dots are spaced 1 μm apart, while the control pulses have wavelength 900–950 nm. Designing such a system would be a formidable challenge, but fortunately it has been achieved already in a mature industry: photolithography for the fabrication of integrated circuits. A typical approach in photolithography is to design an optical mask such that light shined through the mask creates a desired optical profile on an image plane parallel to the mask. Among the various types of masks for manipulating light, a recent technique is the use of phase-shift masking [60, 61]. Rather than blocking or passing light (as in opaque masks), the phase shift mask is transparent everywhere, but the mask consists of regions which impart different phase shifts to the light which passes through. These phase shifts cause interference patterns in the light on an image plane after the mask. Although the optical pulses are broadband compared to monochromatic laser light, the bandwidth is sufficiently narrow that interference patterns are preserved. Development of these phase-shift masks is complex but routine for photolithography, so QuDOS can leverage a well-studied engineering problem to control the optical pattern of light striking the quantum dot array. The phase-shift masks will create an interference pattern which focuses the laser beam to certain target QDs, while the MEMS mirrors can modulate whether the light pulse is sent to a group of QDs.

2.1.6. Quantum Non-Demolition (QND) Measurement The essential measurement operation in QuDOS consists of an optical pulse which uses dispersive quantum non-demolition (QND) readout based on Faraday/Kerr rotation. The underlying physical principle is as follows: an off-resonant probe pulse impinges on a quantum dot, and it receives a different phase shift depending on whether the quantum dot electron is in the spin-up or spin-down state. External photodetectors (section 2.1.7) measure the phase-shift, thereby inducing measurement of the electron spin.

The physics of such a QND measurement has favorable engineering consequences. The fact that the probe pulse is off-resonant means that inhomogeneity among various quantum dots can be tolerated to a higher degree than is true in schemes involving resonant pulses. The technique is simple, and does not require additional "ancilla" quantum dots (or other structures) to be fabricated. Finally, the probe pulse can have a relatively high photon count, resulting in less stringent detector requirements. Several results in recent years have demonstrated the promise of this mechanism for measurement: multi-shot experiments by Berezovsky *et al.* [62] and Atature *et al.* [63] have measured spin-dependent phase shifts in charged quantum dots, and Fushman *et al.* [64] observed a large phase shift induced by a neutral quantum dot in a photonic crystal cavity.

There are however several challenges related to this scheme. First, the measurement must be "single shot" — after just one probe pulse is applied, the measurement result via photodetection is correct with high probability. For a sufficiently large detuning, the ability to complete a single-shot QND measurement depends on the cooperativity factor C of the cavity. For a sufficiently large detuning Δ, the ability to complete a single-shot QND measurement depends only weakly on Δ; the critical factor is the cooperativity factor C. The phase shift in the probe pulse, θ, scales as the detuning, as well as with C. However, the probability for a photon to create a trion state, which decays by spontaneous emission, scales as C/Δ^2 [65]. For an input probe pulse that is in a coherent state, the number of photons required to resolve a phase shift θ scales as $1/\theta^2 \propto \Delta^2/C^2$, indicating that the probability of spontaneous emission during a single-shot measurement (which would spoil its QND character, i.e. introduce measurement error) scales as $1/C$, independent of Δ. Consequently, a large cooperativity factor of the cavity (e.g. $C \sim 10^3$) may allow single-shot dispersive QND measurements to be carried out with low measurement error.

A second challenge with this measurement scheme involves the selection rules of the quantum dot in a magnetic field. The ultrafast single qubit rotation scheme [42] requires a Λ-system for the electron spin, but this is only available when the static magnetic field is applied perpendicular to the semiconductor growth axis (Voigt geometry). Thus far, the multi-shot demonstrations of dispersive QND readout have only been performed with parallel orientation [63] or low strength magnetic fields [62]. The demonstration of single-shot QND measurement in Voigt geometry, with high magnetic fields, is still possible, but the phase shifts are likely to be smaller. Specifically, there are two active Λ-systems which provide competing phase shifts, so only the difference between the two phase shifts can be detected. The actual value of the achievable phase shift will depend on the trion energy structure, which in turn depends on quantum dot growth parameters such as strain and dot ellipticity.

2.1.7. Detector Array To enable parallel operations in QuDOS, measurement must also be performed in a parallel fashion by an array of photodetectors. A measurement light pulse reflected from the cavity is directed to an integrated grid of CMOS imagers, which is an alternative imaging technology to the more common CCD [66]. Additional control circuitry for Layer 3 is also embedded in this array. The surface code quantum error correction implemented in Layer 3 (see section 4.1.3) must process the outcomes of measurement on syndrome qubits to determine correction operations for errors that have occurred. To make this error analysis step fast and efficient, the necessary processors for error correction are integrated with the array of photodetectors.

The requirements for the detectors will partially be determined by how large the phase shift of the dispersive measurement pulse can be made, which is influenced by the cavity and quantum dot parameters. Fundamentally, however, the detectors are used to make a decision on whether an impinging pulse contains an average photon number below or above a certain threshold. Single photon detection capability is thus not important. It may be possible to compensate for poor detector quantum efficiency by increasing the measurement probe power, although higher quantum efficiency is preferable, since the probability of measurement error scales with probe power. The gain curve of the detector and amplifier circuitry is important, since it may be necessary to distinguish between a 1 nanosecond pulse containing, for example, 10^5 photons on average, and a pulse with just 1% more photons on average; the detector must not saturate near the used probe pulse power, and must have sufficient gain at those powers that the small difference in average photon number can be discerned with high probability.

For the expected phase shift, there appears to be no fundamental limitation to engineering a CMOS imaging array that is sufficiently sensitive, fast (GHz operation frequency), and large (one pixel per quantum dot to be simultaneously measured) to meet the requirements for QND readout. Current state-of-the-art CMOS image sensors are not yet advanced enough, especially with respect to speed (frame rate), but rapid progress is being made, driven by commercial requirements in a wide variety of applications [67].

2.1.8. Static Decoherence (Memory Errors) The continuous phase evolution discussed in section 2.1.1 would not pose a problem if it was constant — it could be mitigated by synchronizing pulse arrival times to the Larmor period [52]. However, the nuclei in the vicinity of the quantum dot electron also have nonzero spin, so they interact with the electron by the hyperfine interaction. This creates an effective magnetic field with random orientation and bounded magnitude acting on the electron. The effect is that the phase evolution between the spin levels is different for each quantum dot electron, and difficult to determine. However, the nuclear spins are stable on timescales much longer than the electrons, so that the perturbation to the electron spin is effectively an unknown constant, within the electron $T_2 \sim 1$ μs timescale. This phenomenon is responsible for the ensemble dephasing time (${T_2}^* \sim 1$ ns [68]). This error source obscures the system designer's ability to track the phase evolution of the spin vector on the Bloch sphere, but it is not fatal, as this problem can be addressed by Layer 2 techniques (see section 3). We note also that in some semiconductors, isotopic purification (removing any atoms with nonzero nuclear spin) can improve dephasing times by an order of magnitude [69], but this approach is not possible for QuDOS since there are no stable zero-spin nuclear isotopes of In, Ga or As.

2.1.9. Dynamic Coherent and Incoherent Errors Coherent errors, such as deviation in the axis of rotation or angle of rotation on the Bloch sphere, preserve state population in the two-level spin system (which later serves as the foundation of the virtual qubit). In section 3.2, we illustrate techniques in Layer 2 for addressing systematic coherent errors which occur in the Physical layer.

Incoherent processes involve coupling to modes outside of the two-level spin system, which is problematic because this leads to an irrecoverable loss of quantum information. The broadband pulses induce virtual transitions between the metastable spin levels and the excited trion levels. However, there is a possibility that a real excitation of a trion can occur, such as if the detuning from resonance is too small or a phonon interacts with the system to cause actual absorption of a photon (and generation of a trion). The exciton lifetime in the GaAs system is $T_{1,X} = 1$ ns, so when the trion decays by spontaneous emission, the state of the two-level spin system underpinning our virtual qubit is effectively measured without knowledge of the result, leading to complete depolarization of the qubit.

2.2. Layer 1 Performance

Operational performance is critical when designing a computing system. Execution time and accuracy are particularly important for quantum computers, where expected logical operation speed may play a role in deciding which physical system one chooses. Performance in the physical layer depends on the timing and duration of optical pulses which manipulate the charged QD spin system. Table 1 lists some of the critical parameters for the physical processes required: broadband pulses and precession in the magnetic field are needed for "raw" 1-qubit gate pulses, QND pulses provide spin state measurement, and the entangling operation is the basis of the 2-qubit gate.

2.2.1. Manipulating the Spin-basis Bloch Sphere QuDOS must be able to control the charged quantum dot spin system by rotating the spin state represented by a Bloch vector around two orthogonal axes on the Bloch sphere. This requirement arises because we use this system to construct the "virtual qubit" in Layer 2 (see section 3.1.1), and two separate axes of control are necessary for arbitrary SU(2) operations.

The first way to control the spin state is through the static magnetic field. The spin states are split in energy, so the relative phase between the two levels precesses at the Larmor frequency of about 25 GHz in a 7 T field. This can be viewed as a continuous rotation around the Z-axis on the Bloch sphere.

Stimulated Raman transitions produced by ultrafast broadband optical pulses incident on the quantum dot coherently rotate population between the spin states, which in the idealized Bloch sphere can be interpreted as X-axis rotations. However,

Operation	Mechanism	Duration	Notes
Spin phase precession (Z-axis)	Magnetic field splitting of spin energy levels	$T_{\text{Larmor}} = 40$ ps	Inhomogeneous nuclear environment causes spectral broadening in Larmor frequency, which is the source of $T_2{}^*$ processes.
Spin state rotation pulse	Stimulated Raman transition with broadband optical pulse	$\tau_{\text{pulse}} = 14$ ps	Red-detuned from spin ground state-trion transitions.
Entangling Operation	Nonlinear phase shift of spin states via coupling to a common cavity mode	$\tau_{\text{entangle}} = 100$ ns	CW laser signal modulated by an electro-optic modulator (EOM).
QND Measurement	Dispersive phase-shift of light reflected from planar cavity	$\tau_{\text{QND}} = 1$ ns	CW laser signal modulated by an EOM.

Table 1. Parameters for Layer 1 quantum operations. Spin phase precession is determined by the spin-state energy splitting due to an external magnetic field. To implement a Hadamard gate, the broadband pulse time is $1/\sqrt{8}$ of the Larmor period (T_{Larmor}). Times for entangling operation and QND measurement are estimated from simulation.

there are some important non-ideal effects which must be addressed. A perfect X-axis rotation is only possible in the limit of an infinitely fast pulse, where the spin vector precession (due to the magnetic field) on the Bloch sphere during the optical pulse goes to zero. As we see in Table 1, the Larmor frequency is comparable to the broadband pulse duration. Even very fast pulses (< 1 ps) will still incur significant error, which lowers gate fidelity and increases the burden on Layer 2 to produce gates with error below the threshold of the surface code.

An alternative approach is to tune the broadband pulse amplitude so that the angular velocity of rotation around the X-axis is equal to the velocity of rotation around the Z-axis due to the magnetic field. One can verify that the resulting rotation by an angle π is equivalent to applying a Hadamard gate, which in conjunction with arbitrary Z-rotations from the magnetic field is sufficient to produce any SU(2) gate. Moreover, unlike very fast pulses, this operation can in principle produce high-fidelity state rotation.

2.2.2. Entangling Operation Universal quantum computation requires a gate which generates entanglement. The surface code requires the virtual gate `Controlled-NOT` (`CNOT`) which must come from Layer 2. To produce this gate, Layer 1 must provide a mechanism for generating entanglement between the spins of the charged quantum dots. The method proposed for this architecture (discussed in section 2.1.4) couples two electron spins with a common cavity optical mode. Simulation of this process indicates that it requires a modulated continuous-wave laser pulse about 10–100 ns in duration [44]. The effect of this pulse on the virtual qubits formed by two neighboring charged quantum dots is to induce a non-linear phase shift dependent on the state of the electron spins. This is equivalent to a `Controlled-Z` gate at Layer 2, which can be transformed into the `CNOT` gate with single-qubit operations (in this case, virtual Hadamard gates).

2.2.3. MEMS Micromirror Switching Switching delay for the MEMS mirrors depends on their mechanical properties, which are limited by the fabrication processes and actuation requirements. We anticipate that the switching delay can be reduced to ≤ 1 μs, but that alone is insufficient for controlling the crucial optical signals in QuDOS. Most of the optical signals can be applied in a repeated pattern across the entire array of QDs, but measurement and the associated single-qubit gates to change the basis of measurement must be multiplexed to the appropriate quantum dots. Therefore, this one particular set of operations requires two MEMS mirror arrays (designated "A" and "B" for simplicity) which both couple into a single beamsplitter. Electro-optic modulators (EOMs) control whether laser light signals reach the mirror arrays and reflect to the beamsplitter, which in turn directs light to the QDs. The EOMs alternate which mirror array is "on", by one transmitting light while the other blocks. When A is on, the mirror array is static and a certain measurement pattern is projected onto the QDs for every measurement light pulse. Meanwhile, B is re-positioning its mirrors for the next measurement pattern. When B is ready, the EOMs switch states, and now B is "on" while A re-positions its mirrors for the next measurement pattern. By using *alternating MEMS arrays*, we can overcome the slow switching speed of the MEMS mirror technology.

3. Layer 2: Virtualization

Quantum information systems are very sensitive to imperfections in their environment and control, which manifest as errors in the stored information. These errors can be systematic or random. Layer 2 sharply reduces systematic errors since this can be accomplished without measuring the system state, which is inherently faster and simpler than error-correcting methods which extract information about errors. Quantum error correction is implemented in Layer 3 to correct general errors, but doing so requires syndrome extraction circuits which implement non-local 2-qubit gates and operate at longer timescales. The purpose of Layer 2 is to reduce the error rate in virtual qubits and gates to the levels sufficient for Layer 3 to function.

3.1. Components of the Virtualization Layer

3.1.1. Virtual Qubit The virtual qubit is an abstraction of the underlying physical system. It approximates an ideal qubit as a two-level system whose state is constant until purposefully manipulated. However, the virtual qubit is modeled with real decoherence. In QuDOS, the virtual qubit is created from the two metastable spin states of an electron confined to a QD. The raw physical system has dephasing time ${T_2}^* \approx 1$ ns [68] caused by an inhomogeneous distribution of nuclear spins in the environment of the electron. This dephasing time is insufficient for the Layer 3 operations, and so this system must be augmented with dynamical decoupling (DD) techniques [24, 25], which extend the dephasing time of the virtual qubit into the microsecond regime (see section 3.2.1). Additionally, the electron spin vector precesses with the Larmor frequency about the Z-axis on the Bloch sphere, whereas the virtual qubit is static. This abstraction is achieved by appropriately timing measurement and control optical pulses, as discussed in sections 3.2.1 and 3.2.2.

Measurement of the virtual qubit is achieved by the QND measurement of the spin state from Layer 1 (see section 2.1.6). In principle multiple measurements could be performed in Layer 1 in order to increase measurement fidelity, but this architecture uses single-shot readout for the sake of speed.

3.1.2. Virtual Gates Quantum operations must be implemented by physical hardware which is ultimately faulty to some extent. Many errors are *systematic*, so that they are repeatable, even if they are unknown to the quantum computer designer. In Layer 2, virtual gates manipulate the state of the virtual qubit by combining fundamental control operations in Layer 1 in a manner which creates destructive interference of control errors. Virtual gates must suppress systematic errors as much as possible in order to satisfy the demands of the error correction system (Layer 3). For example, in QuDOS, the ultrafast pulses in Layer 1 would ideally induce a state rotation in the spin basis (two-level system), but inevitably the physical system will suffer from some loss of fidelity by both systematic and random processes. This section explains the theory behind the virtual gate, while section 3.2.2 illustrates how a simple virtual gate scheme is developed in QuDOS.

Efficient schemes exist for eliminating systematic errors. Compensation sequences can correct repeatable (but perhaps unknown) errors in the state rotation operations [26, 27]. This condition is often true since errors are frequently due to imperfections in the Layer 1 processes, such as laser intensity fluctuations over long timescales or the coupling strength of the electron to the optical field (caused by fabrication imperfections). Since these errors are systematic over the timescales of operations in this architecture, a compensation sequence is effective for generating a virtual gate with lower net error than each of the constituent gates in the sequence. Moreover, many compensation sequences are quite general, so that error-reduction works without knowledge of the type or magnitude of error.

3.2. Layer 2 Performance

The Virtualization layer can sharply reduce systematic device errors, but not random errors; therefore, Layer 2 must operate fast enough to permit Layer 3 to correct the remaining random errors. As discussed in section 2.1.8, memory errors accrue over time regardless of what operation is being executed. Layer 2 mitigates memory and control errors, but if the virtualization operations require too long to execute, the residual error will be above the threshold of the surface code, and Layer 3 cannot function. Figure 5 gives a broad view of Layer 2 in QuDOS, and the following subsections give a detailed analysis of its performance.

3.2.1. Virtual Qubit Constructing the virtual qubit requires Layer 2 to conceal the complexity of controlling the QD spin state. The QD electron resides in a strong magnetic environment. The magnetic field induces a splitting of the spin energy levels, causing a time-dependent phase rotation of the spin states. Since the spin levels form the basis of the qubit, this is equivalent to a continuous rotation of the Bloch vector around the Z-axis. Therefore, control pulses must be accurately timed so that they perform the desired operation.

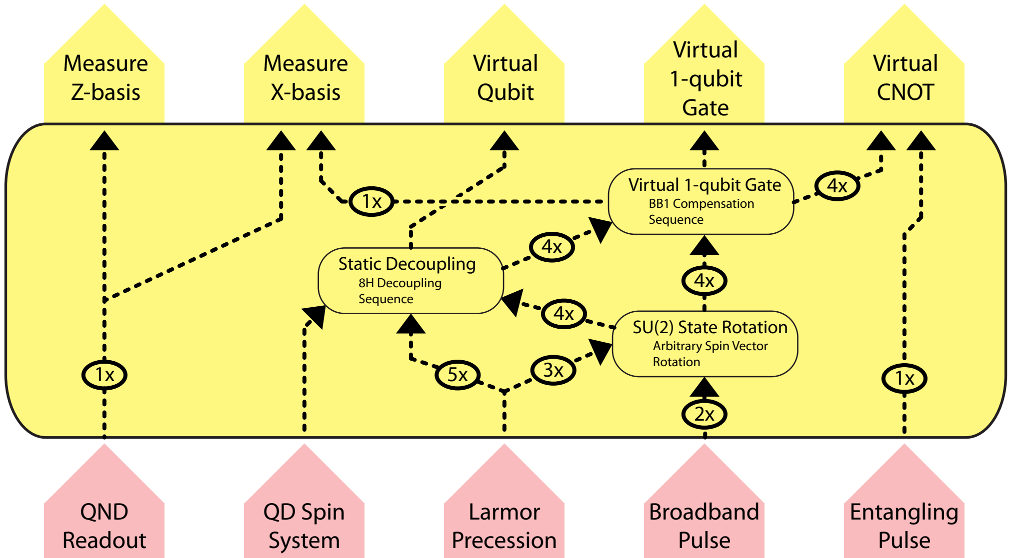

Figure 5. The mechanics of the virtualization layer. The outputs of Layer 1 are combined in controlled sequences to produce virtual qubits and gates. Arrows indicate how the output of one process is used by another process. The circled numbers indicate the quantity of a certain resource being used.

Control of the QD spin is complicated by the inhomogeneous nuclear environment which causes the Z-axis rotation to proceed at a somewhat uncertain angular frequency. This problem is mitigated by a dynamical decoupling sequence, so that the system is decoupled from environmental noise and brought into a precisely controlled reference frame at a predictable time. The sequence in Figure 6 illustrates such a decoupling sequence, appropriate for use in this architecture. Although longer sequences may consist of more pulses, to minimize execution time, we have chosen a sequence of eight Hadamard pulses. Instead of using a more common sequence like Carr-Purcell (CP) [70, 71] or Uhrig dynamical decoupling (UDD) [72], the sequence in Figure 6 is custom designed to eliminate to first order the errors which occur in both the free evolution and control of the virtual qubit (CP and UDD cannot accomplish the latter). We note however that the 8H sequence does have a structure similar to the CP sequence.

The virtual qubit is formed by hiding the details of the inhomogeneous phase angular velocity with the DD sequences. Control and readout pulses are timed to arrive exactly when the DD sequence brings the QD spin state back into focus, so that above Layer 2 the virtual qubit appears to be a static quantum memory.

The definition of the virtual qubit is the subspace spanned by the QD electron spin states, which coincides with the measurement process in Layer 1. The measurement pulse and readout projects the electron into one of the spin states. Measurement of the virtual qubit requires that the DD sequence be halted, because decoupling interferes with measurement. Since the measurement pulse is in the Z-basis, rotations around the Z-axis (from the magnetic environment) do not affect the outcome. Neglecting

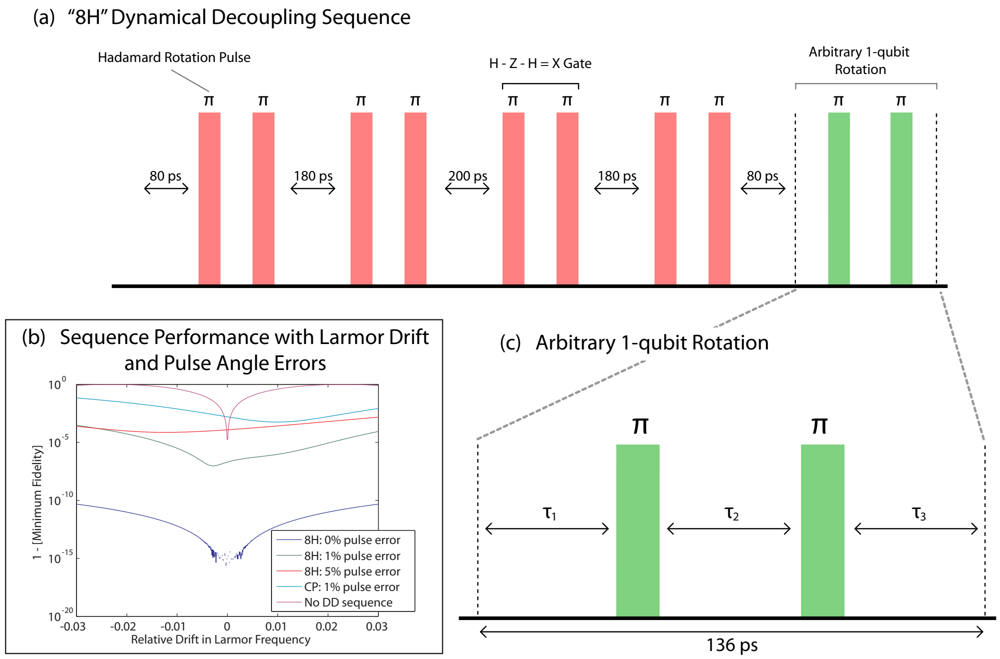

Figure 6. The 8-pulse Hadamard (8H) sequence used in this architecture can eliminate both memory and control errors to first-order. (a) Each bar represents a pulse rotating the Bloch vector by angle π around the axis $\frac{1}{\sqrt{2}}(\hat{X}+\hat{Z})$, which is equivalent to the Hadamard gate. The red bars indicate pulses with fixed arrival times which perform dynamical decoupling. The arrival time of the green bars is varied to produce a desired virtual gate. (b) Simulation of the 8H sequence shows that good performance is possible even with both pulse angle errors and drift in the Larmor frequency at a particular quantum dot. In experiments, the Larmor frequency can drift by about $\pm 2\%$, which is consistent with the result $T_2{}^* \approx 1$ ns [68]. We determine later that based on the threshold of quantum error correcting codes, the error in a virtual gate should be less than 10^{-3}. From simulation, we see that even 5% pulse error in the 8H sequence will reach this performance, whereas 1% pulse error in the CP sequence is insufficient. Not using any dynamical decoupling leads to unacceptable error rates in this system because of the Larmor frequency drift. The simulation runs into a numerical accuracy limit at $\sim 10^{-15}$. (c) Construction of an arbitrary 1-qubit rotation requires 136 ps. The delays τ_1, τ_2, and τ_3 are varied to produce an arbitrary gate. The pulses are Hadamard gates.

DD during measurement is acceptable because the longitudinal (T_1) relaxation time is very long compared with the measurement pulse duration [73, 74].

3.2.2. Virtual Gates Virtual gates manipulate the state of the virtual qubit, but they must use Layer 1 to do so. However, the Layer 1 processes have errors which must be suppressed to form successful virtual gates, which are defined as having error rates tolerable for the error correction in Layer 3 to function. Fortunately, control errors are often systematic, and efficient techniques exist for canceling such errors. This quantum computer uses compensation sequences [26, 27], in which a series of pulses accomplishes the desired gate in such a manner that pulse errors interfere destructively and cancel to first order.

First, let us construct a "raw" gate, which is a sequence of pulses that accomplishes arbitrary SU(2) rotation of the virtual qubit, but without any error suppression. Figure 6(c) provides a template for constructing any such sequence, which requires at most 136 ps in QuDOS. This operation time is determined by the Larmor precession in Layer 1; the quantity is exact since any errors are predominantly systematic and therefore corrected by Layer 2. To deterministically apply the gate we desire, this sequence must coincide with the common reference frame produced by the DD sequence above. For convenience, we select the delays in Table 3 such that the DD sequence combined with an arbitrary SU(2) gate requires 1 ns. One of the simplest compensation sequences (BB1 [26]) requires 4 arbitrary gates; hence the virtual gate (with error cancelation) requires 4 ns.

The virtual 2-qubit gate is accomplished by constructing a `CNOT` gate from the entangling operation in Layer 1 and the virtual 1-qubit gates. The DD sequence is designed so that the Ising-like interaction ($\sigma_z \otimes \sigma_z$) component of controlled-phase rotation is allowed while any 1-qubit phase rotations are suppressed. As a result, the `CNOT` gate can be created by performing 1-qubit virtual gates before and after the entangling operation. However, errors in the entangling operation are due to spontaneous emission [44], which compensation sequences cannot correct; as a result, error in the virtual `CNOT` gate must be suppressed by design of Layer 1 processes as much as possible.

4. Layer 3: Quantum Error Correction

Error correction schemes remove entropy from an information system. In contrast to Layer 2, quantum error correction schemes [28, 75–79] such as the surface code [80] can correct arbitrary errors in the underlying quantum information, assuming the probability of such errors is bounded below a certain threshold [81, 82]. This process of information protection is achieved by continually consuming ancilla states prepared to extract entropy from the quantum computer (via syndrome measurement). Layer 3 of this architecture framework is devoted to quantum error correction (QEC), which is vitally important to the successful operation of the quantum computer.

Layers 2 and 3 are not redundant — they are synergistic. The Virtualization layer cannot correct arbitary errors, and so a large-scale quantum computer will require QEC. However, Layer 2 can mitigate some errors with significantly less effort than would be required in Layer 3, because the Virtualization layer does not extract any information from the system. In this manner, Layer 2 makes Layer 3 more efficient. If errors rates are high, QEC alone may not function at all, and the techniques in the Virtualization layer are essential. The only scenario in which Layer 2 is unnecessary

Operation	**Label**	**Error Cancelation**	**Composition**	**Max Duration**
Hadamard Rotation	H	No	$\frac{1}{2\sqrt{2}}T_{\text{Larmor}}$	14 ps
Z Rotation	$R_Z(\theta)$	No	$\frac{1}{2}T_{\text{Larmor}}$	20 ps
X Rotation	$R_X(\theta)$	No	$H \cdot R_Z(\theta) \cdot H$	48 ps
1-qubit Gate	`1Q`	No	$R_Z(\theta_1) \cdot H \cdot R_Z(\theta_2) \cdot H \cdot R_Z(\theta_3)$	88 ps
Dynamical Decoupling with `1Q`	`DD+1Q`	Yes (T_2)	$\texttt{Delay}(80\text{ ps}) \cdot R_X(\pi) \cdot \texttt{Delay}(180\text{ ps}) \cdot R_X(\pi) \cdot \texttt{Delay}(200\text{ ps}) \cdot R_X(\pi) \cdot \texttt{Delay}(180\text{ ps}) \cdot R_X(\pi) \cdot \texttt{Delay}(80\text{ ps}) \cdot \texttt{1Q}$	1 ns
Virtual 1-qubit Gate	`Virtual1Q`	Yes (T_2 and Gate Error)	$\texttt{DD+1Q}_1 \cdot \texttt{DD+1Q}_2 \cdot \texttt{DD+1Q}_3 \cdot \texttt{DD+1Q}_4$	4 ns
Controlled-NOT	`CNOT`	Partial (T_2 and 1-qubit only)	$\texttt{VirtualH}^{\otimes 2} \cdot \texttt{Controlled-Z} \cdot \texttt{VirtualH}^{\otimes 2}$	100 ns
Z-basis Measurement/ Initialization	`MZ/IZ`	-	τ_{QND}	1 ns
X-basis Measurement	`MX`	-	$\texttt{VirtualH} \cdot \texttt{MZ}$	5 ns
X-basis Initialization	`IX`	-	$\texttt{MZ} \cdot \texttt{VirtualH}$	5 ns

Table 2. Virtualization Layer Operations

(and perhaps harmful) is if the errors in the Physical layer are completely uncorrelated, in which case Layer 2 control techniques yield no benefit. In QuDOS, systematic errors dominate (as witnessed by the fact that ${T_2}^*$ is at least three orders of magnitude shorter than T_2 [68]), and so Layer 2 is critical to this architecture.

Within QuDOS, our specific architecture implementation, the surface code is the crucial means to provide logical qubits and gates with the exceptionally low error demanded of a large-scale quantum algorithm such as Shor's factoring algorithm. We will not review the entirety of the surface code here, but instead refer the interested reader to several key works in the field [29, 83, 84]. This section is devoted to the important architecture-related matters of surface code QEC, such as resource requirements in terms of Layer 2 outputs (virtual gates and qubits) and time to implement logical operations.

4.1. Components of the QEC Layer

The QEC layer uses error correction to provide fault-tolerant logical qubits, logical gates, and logical measurement to Layer 4. We explain the salient aspects of the surface code, the error correction scheme in QuDOS, but in general the processes in Layer 3 can vary significantly between different forms of QEC. The surface code provides the ability to correct arbitrary errors with quantum error correction [29, 83, 84]. Virtual qubits in a broad 2-dimensional array are encoded into a single surface code via single-qubit operations and nearest-neighbor (`CNOT`) gates. Logical qubits are produced by forming "defects" in the surface code. A defect is a rectangular connected region of virtual qubits in the lattice which have been measured, so that the resulting surface code lattice has an SU(2) subspace of freedom, equivalent to a qubit. Ref. [29] gives an overview of the steps needed to construct the surface code. For practical matters (explained in Ref. [84]), a logical qubit is constructed from two defects. In contrast to Layer 2, the surface code gathers information on the system state by periodically measuring an error syndrome and using this knowledge to correct errors in post-processing. The probability of an undetected error decreases exponentially as a function of the "distance" [85] of the code, so that logical qubits and gates with arbitrarily low error are possible with a sufficiently large code. However, the virtual qubits and gates must have error rates below the threshold of the surface code (1.4% [86]), so that often error-reduction techniques in Layer 2 are necessary for Layer 3 to function. The error rate in virtual qubits and gates needs to be about an order of magnitude below the threshold, or approximately 10^{-3}, for the surface code to be manageable in size.

4.1.1. Architecture and the Surface Code In contrast to some other QEC schemes, the surface code has some key advantages for architecture. In particular, the surface code requires only local and nearest-neighbor gates between qubits in a square lattice. Within this architecture framework, the necessary Layer 2 components for the surface code to function are the injection of single-qubit states needed for non-Clifford gates, a two-dimensional array of qubits with nearest-neighbor coupling (`CNOT`), and measurement in the X and Z bases [29, 87]. The two-dimensional arrangement with nearest-neighbor `CNOT` gates is most readily achieved in QuDOS with a physical 2D array of quantum dots, each supporting a virtual qubit. Although the single-qubit Pauli rotations are needed to form a complete set for universal quantum computation, we may neglect these in the present context by simply maintaining a continually-changing Pauli frame in a classical computer and modifying the final measurement results of the quantum computation [88].

4.1.2. Pauli Frames A Pauli frame [88,89] is a simple and efficient classical computing technique to track the result of applying a series of Pauli gates (X, Y, or Z) to single qubits. The Gottesman-Knill Theorem implies that tracking Pauli gates can be done efficiently on a classical computer [90]. Many quantum error correction codes, such as the surface code, project the encoded state into a perturbed codeword with erroneous single-qubit Pauli gates applied (relative to states within the codespace). The syndrome reveals what these Pauli errors are, and error correction is achieved by applying those same Pauli gates to the appropriate qubits (since Pauli gates are Hermitian and unitary). However, quantum gates are faulty, and applying additional gates may introduce more errors into our system.

Rather than applying every correction operation, one can keep track of what correction operation *would be applied*, and continue with computation. As stated above, this is permitted for the case of Pauli gates. When a measurement is finally made on a qubit, the result is modified based on the corresponding Pauli gate which should have been applied earlier. This stored Pauli gate is called the Pauli frame [88, 89], since instead of applying a Pauli gate, the quantum computer *changes* *the reference frame for the qubit*, which can be understood by remapping the axes on the Bloch sphere, rather than moving the Bloch vector. The quantum computer operations proceeds normally, with the only change being how the final measurement of that qubit is interpreted.

We emphasize that the Pauli frame is a *classical object* stored in the digital circuitry which handles error correction. Pauli frames are nonetheless very important to the functioning of a surface code quantum computer. Layer 3 uses a Pauli frame with an entry for each virtual qubit in the lattice. As errors occur, the syndrome processing step identifies a most-likely pattern of Pauli errors. Instead of applying the recovery step directly, the Pauli frame is updated in classical memory. The Pauli gates form a closed group under multiplication (and global phase of the quantum state is unimportant), so the Pauli frame only tracks one of four values — X, Y, Z, or I — for each virtual qubit in the lattice.

4.1.3. Measurement and Detector Arrays As we saw in Layers 1 and 2, the grid of QDs facilitates the nearest neighbor entangling operations for a virtual CNOT gate. Measurement is also done in an array fashion, with a corresponding lattice of photodetectors. This detector array also functions in Layer 3 since the measurement results must be processed at the surface code level. Rather than sending the multitude of measurement results to a separate location (and incur the delays and communication bottlenecks), the surface code error syndrome processors are co-located on-chip with the detectors. This is permitted because we can designate some defects in the surface code as stationary while also never needing to measure the virtual qubits there, so that there is a "shadow" on the detector array. We can use this space for digital logic to process measurement results rather than unused photodetectors. The action of these processors is discussed in sections 4.2.3 and 4.2.4.

4.2. Layer 3 Performance

The primary purpose of Layer 3 is to produce logical qubits and gates with arbitrarily low error from the faulty virtual qubits and gates. For this reason, accuracy is the primary performance figure of Layer 3. Assuming 100% yield and independent error sources, any desired logical (Layer 4) accuracy can be achieved, provided that: (a) the Layer 2 operations have error below the Layer 3 threshold (1.4% for the surface code [86]); and (b), the quantum computer has sufficient space in terms of virtual qubits to host a QEC code as large as necessary. For the purposes of QuDOS in this investigation, we assume that both requirements are achievable and analyze the resources needed to realize such a surface code quantum computer. However, we will show that requirement (b) can be very demanding since realistic hardware will have error rates which require very large surface codes. After establishing the space requirements of a fault-tolerant quantum computer architecture (with a specified arbitrary accuracy), we then analyze the time needed to execute Layer 3 operations, which will ultimately determine the logical "clock speed" or operation frequency of the quantum computer in Layer 4. Figure 7 provides a schematic view of the processes inside Layer 3.

4.2.1. Size of the Surface Code Quantum error correction schemes generate protected codespaces within a larger Hilbert space formed from an ensemble of qubits. The tradeoff is that instead of a single qubit, the quantum computer now requires many

Parameter	Symbol	Value
Threshold error per virtual gate	$\varepsilon_{\text{thresh}}$	1.4×10^{-2}
Error per virtual gate	ε_{V}	1×10^{-3}
Logical circuit depth (in lattice refresh cycles)	K	3.4×10^{11}
Number of logical qubits ("Shor", section 5.2)	Q	12288
Error per lattice refresh cycle	ε_{L}	2.7×10^{-18}
Surface code distance	d	27
Virtual qubits per logical qubit	`VQ/LQ`	4830

Table 3. Parameters Determining the Size of the Surface Code in QuDOS

virtual qubits to produce a logical qubit. The number of virtual qubits required for a single logical qubit is an important resource-usage quantity, and it depends on the performance aspects of the quantum computer:

- error per virtual gate (ε_{V}), which is an input to Layer 3 from Layer 2
- threshold error per virtual gate of the surface code ($\varepsilon_{\text{thresh}}$)
- distance (d) of this instance of the surface code
- error per logical gate (ε_{L}), which is upper-bounded by the performance requirements of the quantum algorithm in Layer 4

To determine ε_{L}, the simplest approach ("KQ product") assumes the worst case. If the quantum algorithm has a circuit with logical depth K acting on Q logical qubits, then the maximum failure probability is given by

$$P_{\text{fail}} = 1 - (1 - \varepsilon_{\text{L}})^{KQ} \approx KQ\varepsilon_{\text{L}} \tag{1}$$

for small ε_{L}. Therefore, we demand that $\varepsilon_{\text{L}} \ll 1/KQ$. Given these quantities, the average error per logical gate in the surface code may be closely approximated [85] by

$$\varepsilon_{\text{L}} \approx C \left(\frac{\varepsilon_{\text{V}}}{\varepsilon_{\text{thresh}}} \right)^{\lfloor \frac{d+1}{2} \rfloor} \tag{2}$$

where C is a constant determined by the implementation of the surface code. The data in Ref. [85] suggests $C \approx 3 \times 10^{-2}$. Therefore, given a known ε_{V}, $\varepsilon_{\text{thresh}} = 1.4 \times 10^{-2}$, and $C \approx 0.03$, one can determine the necessary distance d such that the probability of failure of an entire quantum algorithm is sufficiently small. Table 3 provides an example of these calculations for the QuDOS quantum computer. Error per virtual qubit (ε_{V}) is also assumed, and the K and Q values are for Shor's algorithm factoring a 2048-bit integer (see section 5.2). We have assumed $\varepsilon_{\text{L}} \leq 10^{-2}/KQ$, so that the success probability of the quantum algorithm is greater than 99%.

Determining the necessary distance for the surface code allows one to compute the minimum number of virtual qubits needed to produce one logical qubit, which consists of two defects separated from each other and any other defects or boundaries by the distance of the code. Table 3 calculates this number for QuDOS, but we emphasize that a complete surface code quantum computer will need additional virtual qubits to facilitate movement of defects (braiding) and the distillation of singular qubits needed for non-Clifford logical gates. As a result, the total number of virtual qubits from Layer 2 — and therefore the number of quantum dots from Layer 1 — is larger than simply the product of [*virtual qubits per logical qubit*] $\times$ [*logical qubits*].

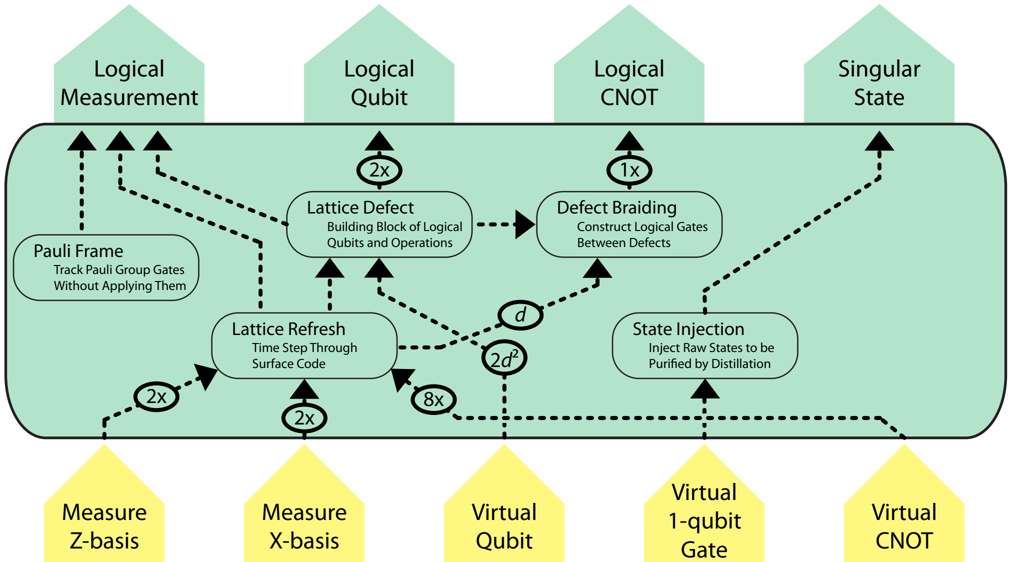

Figure 7. Process translation in Layer 3. A surface code is constructed with virtual qubits and gates, ultimately yielding logical qubits and operations. The arrows in yellow along the bottom are outputs of Layer 2, whereas the green arrows at the top are the outputs of Layer 3. Small dashed arrows indicate that the output of one process is used by another process. The circled number is the quantity of the corresponding resource which is used.

Accounting for these additional virtual qubits is crucial to accurately estimating the resource requirements for QuDOS. More generally, the quantity of these additional qubits depends significantly on the algorithm one is implementing, since the number of singular qubits is related to the types of logical gates one must implement. A total accounting of the virtual qubits in the surface code is given in section 5.2.

4.2.2. Surface Code Operations in Time The fundamental time step in Layer 3 is one unit along the simulated time axis of the topological cluster state [87], which is the lattice refresh cycle of the surface code. Within this architecture, the virtual gates needed for this process are performed in parallel across the entire array of virtual qubits. This parallelism is a fundamental strength of the architecture, because the lattice refresh time can be very fast as shown in Table 4. Moreover, refresh time is independent of system size since all operations proceed in parallel; by contrast, in the architecture in Ref. [22], lattice refresh time depends on the size of one axis of the lattice.

Logical qubits in the surface code are defects in the lattice [29], and logical operations involve braiding these defects through simulated time. Figure 7 illustrates how functions of the surface code are constructed from Layer 2 services. For error-correction purposes, the speed of a braiding operation is constrained by the distance of the code, so that if the minimum spatial separation of defects is 27 virtual qubits (as in Table 3), the time to perform braiding must also take at least 27 lattice refresh cycles. This is because the error chains in the surface code can span both spatial and

Operation	**Label**	**Composition**	**Max Duration**
Lattice Refresh with *alternating MEMS arrays*	`LatticeRefresh`	$2 \times (\texttt{IZ} \cdot 4 \times \texttt{CNOT} \cdot \texttt{MZ} \cdot \texttt{IX} \cdot 4 \times \texttt{CNOT} \cdot \texttt{MX})$	1.61 μs
Defect Braiding	`DefectBraid`	$27 \times$ `LatticeRefresh`	43.5 μs
Logical CNOT	`LogicalCNOT`	`DefectBraid`	43.5 μs

Table 4. Layer 3: Surface Code Operations

temporal dimensions, with units along the time axis defined by the lattice refresh time. As such, any defects must be separated by distance d in time and space within the surface code. Table 4 shows the time required for several Layer 3 processes including the construction of logical gates such as `CNOT`.

4.2.3. Local Error Correction Processing The error syndrome decoding process in Layer 3 requires the location of error chain endpoints and the subsequent matching of these endpoints into a minimum-weight set of error chains [29, 85, 87]. Section 4.1.3 suggested a method for integrating local surface code processors into the photodetector array. Devitt *et al.* describe how to split the syndrome decoding problem into smaller manageable chunks [20], an approach which is supported by the use of local error correction processors. Nevertheless, minimum-weight matching can require a significant number of calculations, so even special-purpose processors may require a substantial amount of time to complete this task. If latency and classical processing cause significant delay of the availability of the logical measurement result, future logical operations depending on the result can be delayed with logical identity gates. This is computationally reasonable as a linear increase of the size of the logical qubit results in only polynomial increase of the classical processing time but an exponential increase of the logical qubit lifetime, implying arbitrary delay can be handled with only logarithmic overhead. As a result, Layer 3 must signal to Layer 4 when error syndrome processing requires more time, so that Layer 4 inserts the necessary logical identity gates into the sequence of logical operations.

4.2.4. Pauli Frames in Action In this architecture, Pauli frames are dynamic objects, just like a virtual qubit. However, unlike virtual qubits, they are entirely *classical* objects, since they carry two bits of classical information for each qubit to which they apply. For this reason, they exist in the digital circuitry associated with error syndrome processing, since these same processors determine what the Pauli frame should be.

The manner in which a Pauli frame is implemented could be compared to a classical parity mask. Imagine there is a string of data bits, and one has determined where in this string some bits were flipped by errors. This error correction information is stored in a second bit string (parity mask), which consists of 1s where bit-flip errors occurred, and 0s elsewhere. The recovery operation is then the bitwise `XOR` of the two strings. Returning to our quantum computer, Layer 3 will continually record the results of the syndrome measurement step. Before any operation requiring logical measurement (such as a non-Clifford gate), any errors which have occurred must be identified. A parity mask for the entire surface code is created, with an entry for each virtual qubit. The minimum weight matching algorithm processes the accumulated syndrome information and pinpoints the locations of X errors; the parity mask is then updated by flipping the existing entry corresponding to each X error. Note that after this update process, it is possible that a virtual qubit will have experienced two X errors at different times, which cancel each other. The parity mask appropriately has a 0 entry in this event. Complementary to the identification of X errors, a similar procedure is performed for Z errors in a second parity mask. The combination of the X and Z parity masks is the Pauli frame for Layer 3.

The Pauli frame comes into action whenever a logical measurement is made on a pair of defects in the surface code. The individual virtual qubit measurements are modified based on the Pauli frame in Layer 3. If the measurement basis applied at each virtual qubit commutes with the corresponding Pauli frame entry, the measurement result is unchanged. If the measurement anti-commutes with current Pauli frame entry at this virtual qubit, then the measurement result is flipped. This action is comparable to the bitwise `XOR` mentioned above for a classical bit string. Note that the presence of both an X and Z error in the Pauli frame is tantamount to a Y error, as global phase is irrelevant to measurement outcome. After the adjusted measurement result is reported, the corresponding Pauli frame entry is reset to I (0 entry for both X and Z masks). We emphasize that the error *syndrome* in Layer 3 is not identical to the Pauli frame. Using the minimum weight matching algorithm, Pauli frames (corresponding to the identified locations of errors) are determined based on the syndrome, which is the location of error chain endpoints without explicit knowledge of the error chains themselves.

5. Layer 4: Logical

The Logical layer transforms the outputs of the QEC layer into a complete substrate for quantum computing which is used by the Application layer. The QEC layer provides logical qubits and a limited set of logical gates; however, the Application layer may request any arbitrary quantum gate, and it is the task of Layer 4 to create this gate. A specific implementation of the Logical layer depends on what services Layer 3 provides. We develop Layer 4 in the context of using the surface code in Layer 3, which provides logical qubits, logical `CNOT`, and injected singular states. In another quantum computer where the QEC layer provides different outputs, a different set of processes in the Logical layer may be needed.

5.1. Functions of the Logical Layer

The function of the logical layer is to provide the logical qubits and gates needed for the quantum algorithm in the Application layer. The surface code produces logical qubits and gates with arbitrarily high accuracy. However, the only fault-tolerant gates provided by the surface code are the Pauli 1-qubit gates (trivially performed by updating the Layer 4 Pauli frame), initialization and measurement in the X and Z bases, the CNOT gate and the identity gate. Rotations about the X and Z Bloch sphere axes can be achieved given ancilla states of the form $\frac{1}{\sqrt{2}}\left(|0\rangle + e^{i\theta}|1\rangle\right)$, which can be created using non-fault-tolerant techniques. For $\theta = \pi/2, \pi/4$, fault-tolerant state distillation circuits can be used to obtain arbitrarily high fidelity ancilla states enabling arbitrarily high fidelity rotations of these angles. Similar techniques can be used to create ancilla states enabling Toffoli to be implemented. By the Solovay-Kitaev theorem [91], these gates are sufficient to efficiently approximate arbitrary single-qubit logical unitary gates.

Logical Pauli Frame Just as in Layer 3, it is unnecessary to implement logical Pauli gates. Instead, a second Pauli frame exists in Layer 4 which functions exactly like its counterpart in Layer 3 (see sections 4.1.2 and 4.2.4). Whenever a logical Pauli gate would be applied, the corresponding entry in the Layer 4 Pauli frame is parity flipped instead. However, the performance requirements of this Pauli frame are not as strict as the one in Layer 3, so the Logical Pauli frame can exist in software which controls the Logical layer, instead of dedicated hardware as is necessary for the Pauli frame in Layer 3. This can be seen in Table 4, where the fastest rate one would need to apply Logical Pauli gates is after each round of defect braidings, or once every 56.4 μs, and the number of entries in the Layer 4 Pauli frame corresponds to logical qubits, which is 12288. Conversely, the Pauli frame in Layer 3 must be updated every lattice refresh cycle (1.61 μs), and the number of entries is the number of virtual qubits in the surface code: 9.04×10^8, as calculated below in section 5.2. Conventional computers can handle the workload of the Layer 4 Pauli frame in software, but the workload of the Layer 3 Pauli frame demands the custom-designed processors described in sections 4.1.3 and 4.2.3.

5.2. Layer 4 Performance

The Logical layer supports the Application layer, and so we analyze the resources in Layer 4 for the specific purpose of executing Shor's algorithm in Layer 5. The number of logical qubits for Shor's algorithm depends on the particular implementation of the algorithm [6, 92–94]. The algorithm adopted for this quantum computer architecture scales as $\sim 6N$, where N is the number of bits in the number to be factored [95], so that factoring a 2048-bit number requires approximately 12288 logical qubits. However, auxiliary logical qubits are also needed for state distillation (explained in section 5.2.1) required for the Toffoli gates used in the modular exponentiation step of Shor's algorithm (see also section 5.2.2). To factor a 2048-bit number, approximately 90000 logical qubits is sufficient [22]; fewer qubits can be used at the expense of time, since the Toffoli gate operations would be delayed until the injected states are distilled. Additionally, "wiring space" is added for the surface code to enable defects to move and braid when necessary, which is estimated as a 25% overhead in the size of the surface code. With these figures in place, we can estimate the resources required for this quantum computer, as shown in Table 5.

5.2.1. Singular State Distillation Singular qubit states described in section 5.1 are necessary to produce arbitrary logical gates in Layer 4. These singular qubits can be produced by magic state distillation [29, 96]. This process consumes a great deal of resources in the quantum computer since many logical qubits are used for distillation. If states are injected with an approximate error of 0.1%, then distilling a $|Y\rangle$ state ($\theta = \pi/2$) requires two levels of distillation, or at least 49 injected states, to produce one logical $|Y\rangle$ qubit with infidelity (error) of 2.4×10^{-24}. Using one level of distillation is insufficient because the resulting error in the qubit is 7.0×10^{-9}, which is much greater than the logical error rate ($\varepsilon_{\mathrm{L}} = 9.8 \times 10^{-19}$, see section 4.2). Similarly, distilling an $|A\rangle$ state ($\theta = \pi/4$) requires at least two levels of distillation, or at least 225 injected $|A\rangle$ states, to produce one logical $|A\rangle$ qubit with infidelity (error) of

Resource	**Label**	**Composition**	**QuDOS Quantity**
Application Logical Qubits	`AppQubits`	$6\times$ [*bit size of number to be factored*]	12288
State Distillation Qubits	`DistQubits`	(Determined by algorithm)	78000
Size of the Surface Code in Virtual Qubits		$1.25 \times$ `VQ/LQ` $\times$ (`AppQubits` + `DistQubits`)	9.04×10^8

Table 5. Layer 4 Resources in Terms of Logical Qubits and the Corresponding Size of the Surface Code in Virtual Qubits

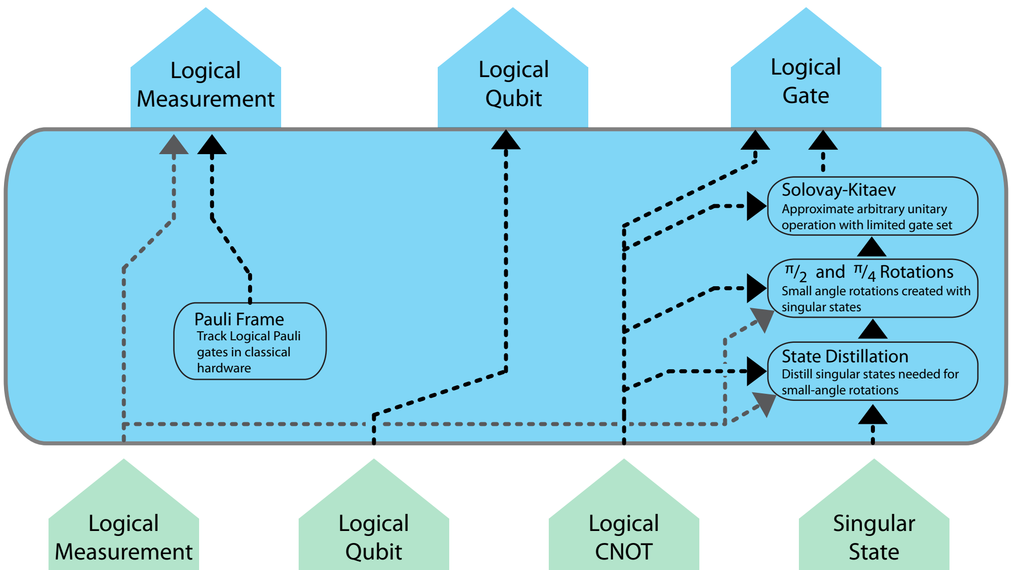

Figure 8. Organization of processes in the Logical layer. Logical qubits from Layer 3 are unaltered, but faulty singular states are distilled into high-fidelity states $|Y\rangle = \frac{1}{\sqrt{2}}(|0\rangle + i|1\rangle)$ and $|A\rangle = \frac{1}{\sqrt{2}}\left(|0\rangle + e^{i\frac{\pi}{4}}|1\rangle\right)$. The distilled states are used to create arbitrary gates with the Solovay-Kitaev algorithm.

1.5×10^{-21}. Consequently, distillation must be performed continuously in parallel with other logical operations to ensure that these purified states are available on demand. Ref. [84] discusses the resource cost and error scaling of this process in more detail. It is noteworthy that distillation is probabilistic, but the probability of success is high for high-fidelity injected states. We assume the injected states are formed from an initialized virtual qubit and one virtual gate. Since the production of these qubits is critical to the performance of a surface code quantum computer, the injection operations in Layers 1 and 2 should be optimized so that distillation converges to a high-fidelity logical qubit quickly.

Operation	Quantity in QuDOS
Toffoli Gate Time	600 μs
`ModExp` Circuit Depth (Toffoli Gates)	7.38×10^8
Minimum Execution Time for Shor's Algorithm	6 days

Table 6. Layer 5 Performance for Shor's Algorithm factoring a 2048-bit number.

5.2.2. Construction of a Toffoli Gate A construction of the Toffoli gate is given in Ref. [23] on p. 182. The small-angle phase and $\pi/8$ gates require singular qubits, as described in Ref. [29]. We will assume here that these singular qubits are distilled as needed, but accurately accounting for the braiding operations and volume of the surface code required for singular state production is an active area of research. Hence we account for the time required to implement a Toffoli gate in terms of the number of braiding steps (the depth of this circuit) assuming the singular states are available. There is one braiding for each gate, giving a total of 13 braidings. This implies a minimum Toffoli gate time of 600 μs.

5.2.3. Summary of Logical Layer Performance We do not calculate the time required to implement any arbitrary gate within the Logical layer, but the prescription is straightforward:

- Specify each logical gate and its accuracy tolerance.
- Use the Solovay-Kitaev algorithm [91] to determine a sequence of available gates from the surface code or state distillation which accurately approximates the desired logical gate.
- Decompose this sequence of gates into the necessary braiding operations, and calculate the total time required.

For Shor's algorithm, the modular exponentiation subroutine (`ModExp`) is the bottleneck to performance. The `ModExp` process depends principally on the Toffoli gate, so we use this figure to estimate the run-time of Shor's algorithm in section 6.

6. Application Layer

The Application layer hosts the quantum algorithm, such as Shor's algorithm [97], that a classical user wishes to execute. Logical gates constructed in Layer 4 are performed on the logical qubits provided by the QEC layer, and the end result is communicated to the classical user. The Application layer is completely unaware of the underlying hardware, since it interfaces only with Layer 4. Since the lower layers have provided all the resources for quantum computing, the figures of merit in Layer 5 are the number of available qubits and the speed of logical operations, which implies the time required to implement a certain quantum algorithm. The size of QuDOS in terms of both virtual and logical qubits was given in Table 5, and the run-time for Shor's algorithm factoring a 2048-bit number is given in Table 6.

We must note however that Table 6 gives a minimum execution time, which can be slowed by some processes we have not fully analyzed here. If the syndrome decoding process in Layer 3 takes longer than expected, non-Clifford operations, such as gates which require singular states, will be delayed. Additionally, we have not yet accurately

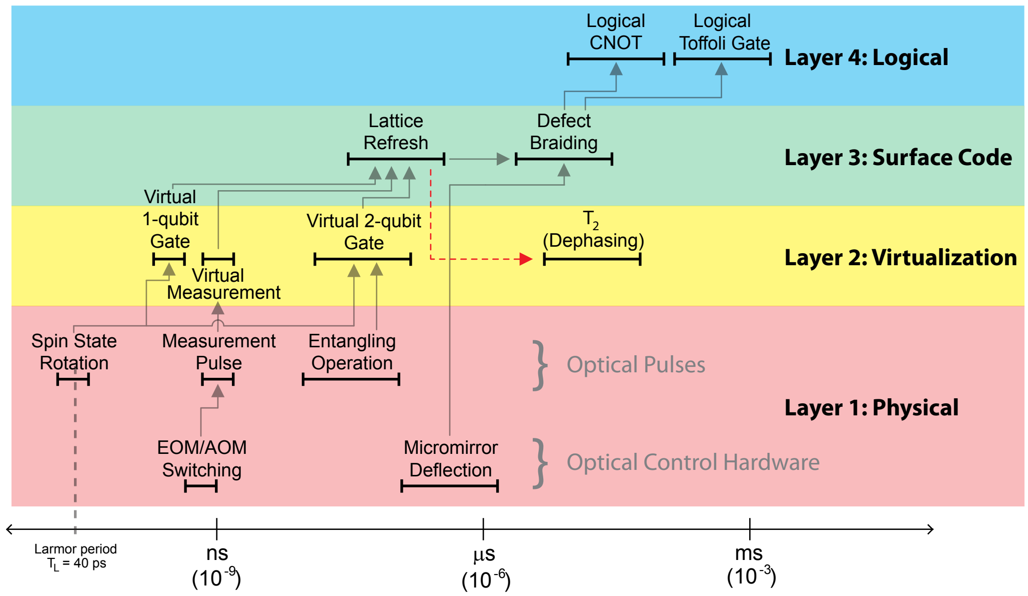

Figure 9. Relative timescales for critical operations in QuDOS within each layer. The arrows indicate dependence of higher operations on lower layers. The red arrow signifies that the surface code lattice refresh must be much faster than the dephasing time in order for error correction to function. The Application layer is not included here since quantum algorithms can vary widely in the time they take to implement, while this figure is concerned with the fundamental operations in a quantum computer.

simulated the braiding operations for the singular state distillation in Layer 4. If this procedure requires more time or space in the surface code than estimated above, then the overall algorithm run-time will suffer. Finally, connectivity is a related issue. We assumed in section 5.2 a 25% overhead, but perhaps more is necessary or long-range interactions in the surface code will become bottlenecks. These matters are the subject of future work.

7. Timing Considerations

Precise timing and sequencing of operations are crucial to making an architecture efficient. In the framework we present here, an upper layer in the architecture depends on processes in the layer beneath, so that logical gate time is dictated by surface code operations, and so forth. This system of dependence of operation times is depicted in Figure 9. The horizontal axis is a logarithmic scale in the time to execute an operation at a particular layer, while the arrows indicate fundamental dependence of one operation on other operations in lower layers.

Examining Figure 9, one can see that the timescales increase as one goes to higher layers. This is because a higher layer must often issue multiple commands to layers below. For example, the virtualization layer must construct a virtual 1-qubit

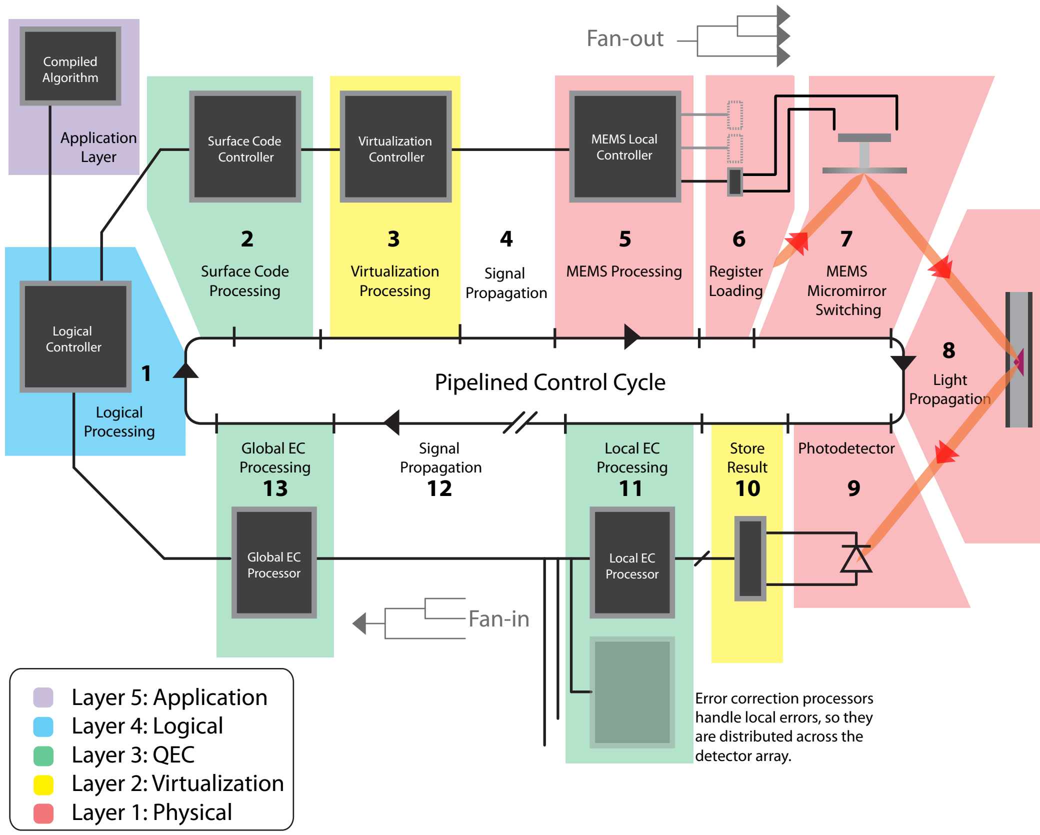

Figure 10. Primary control cycle of QuDOS. Though presented as a sequence of steps, each layer issues multiple commands to the layer below, and operations are pipelined. Each of the numbered steps represents a process whose time duration must be precisely determined in order for the architecture to function efficiently. Steps 4 and 12 indicate significant delays in the propagation of a control or readout signal.

gate from a sequence of spin-state rotations. This process includes the duration of the laser pulses and the delays between pulses, which all add together for the total duration of the virtual gate. Figure 10 shows the QuDOS control loop, which is a more detailed rendition of Figure 2. Here one can see how the essential operations in the architecture interact. In particular, the error syndrome decoding step in Layer 3 is separated into two components, with local processors (described in section 4.2.3) handling small subsections of the surface code while a global processor integrates the results of the local processors into one consistent error pattern. In particular, the global processor corrects any logical measurements based on the Layer 3 Pauli frame (sections 4.1.2 and 4.2.4). The processors in steps 1, 2, and 3 of Figure 10 coordinate the operations in the corresponding layers of the architecture.

The switching delay of 1 μs means that one set of MEMS mirrors cannot multiplex all of the laser pulses in this architecture. Witness in Figure 9 that virtual 1-qubit gates and measurement must operate much faster than this delay permits. Therefore, two micromirror arrays are needed for the crucial measurement operations in Layer 1 and the associated single-qubit virtual gates which change the basis of measurement. As explained in section 2.2.3, one mirror array is used to multiplex light signals while the second is re-positioning. When the second mirror is in place, the electro-optic modulators switch so that the second array multiplexes light while the first re-positions. In this manner, the relatively slow switching delay of the MEMS mirrors can be circumvented, at the expense of losing some optical power.

8. Discussion

We have presented a layered framework for a quantum computer architecture. The layered framework has two major strengths: it is *modular*, and it facilitates *fault-tolerance*. The layered nature of the architecture hints at modularity, but the defining characteristic of the layers we have chosen is encapsulation. Each of the layers has a unique and important purpose, and that layer bundles the related operations to fulfill this purpose. Since technologies in quantum computing will evolve over time, layers may need replacement in the future, and encapsulation makes integration of new processes a more straightforward task. Fault-tolerance is at present the biggest challenge for quantum computers, and the organization of layers is deliberately chosen to serve this need. Arguably, Layers 1 and 5 define any quantum computer, but the layers in between are devoted exclusively to fault-tolerance in an intelligent fashion. Layer 2 uses simple control without monitoring qubit states to mitigate systematic errors, so this layer is positioned close to the Physical layer where techniques like dynamical decoupling and decoherence-free subspaces are most effective. Layer 3 hosts quantum error correction (QEC), which is essential for large-scale circuit-model quantum computing on any hardware, such as executing Shor's algorithm on a 2048-bit number. There is a significant interplay between Layers 2 and 3, because Layer 2 enhances the effectiveness of Layer 3, which is discussed further in section 4. Finally, Layer 4 fills the gaps in the gate set provided by Layer 3 to form any desired unitary operation to arbitrary accuracy, thereby providing a complete substrate for universal quantum computation in Layer 5.

QuDOS, a specific hardware platform we introduce here, demonstrates the power of the layered architecture concept, but it also highlights a promising set of technologies for quantum computing, which are particularly noteworthy for the fast timescales of quantum operations, the high degree of integration possible with solid state fabrication, and the adoption of several mature technologies from other fields of engineering. The operation times for fundamental quantum gates are discussed in section 2, but the importance of these fast processes becomes clear in Figure 9, where the overhead of virtual gates in Layer 2 and QEC in Layer 3 increases the time to implement quantum gates from nanoseconds in the Physical layer to milliseconds in the Logical layer, or six orders of magnitude. In this context, a quantum computer needs very fast physical operations.

Much like their classical counterparts, quantum computers need to scale to large size in order to solve useful problems. In fact, when error correction is included, a quantum computer requires sizable classical processing as well. As with the integrated circuit (IC) industry, integrated fabrication is one of the best methods to solve this dilemma. QuDOS is particularly well-suited to device integration since the quantum memory resides in charged quantum dots, which are formed by solid-state fabrication methods inherited from the semiconductor field. Likewise, the MEMS mirrors and photodetector arrays are also designed to be fabricated with very large-scale integration (VLSI). This approach is proven and robust, and the state of the art is continually being advanced for reasons outside of quantum computing.

The QuDOS architecture has been designed to take advantage of existing mature technologies wherever possible. Doing so allows the architecture to benefit from advances in technology due to other fields of research. For example, the projection optics and phase-shift masking were developed for photolithography in the IC industry. MEMS micromirrors were invented to multiplex light signals in high-definition televisions and projectors. Utilizing these established technologies reduces the burden on quantum computing engineers.

An area which requires further development is the optical engineering in this system. The development of phase-shift masks is routine in photolithography, but it is still very computationally demanding. Moreover, adapting this technique to the current system is complicated by the beamsplitters and MEMS mirrors along the optical paths, as well as the spectral width of the pulses and how they interact with the quantum dots in the planar cavity. Additionally, focusing the laser light signals to the quantum dot array may require a projection optics system, which we have not studied here. Similarly, while integrating logic with photodetectors is feasible, determining the complexity of custom circuits for the syndrome processing step in the surface code is an area of future work. Moreover, integrating digital logic with high-gain photodetectors needed in the context of QuDOS may also present challenges we have not analyzed here.

One of our principle objectives is to better understand the resources required to construct a quantum computer which solves a problem intractable for classical computers. Common figures of merit for evaluating quantum computing technology are gate fidelity, operation time, and qubit coherence time. This investigation goes further to show how connectivity and classical control performance are also crucial. Designing a quantum computer requires viewing the system as a whole, such that tradeoffs and compatibility between component choices must be addressed. A holistic picture is equally important for comparing different quantum computing technologies, such as ion traps or optical lattices. This work illustrates how to approach the complete challenge of designing a quantum computer, so that one can adapt these techniques to develop architectures for other quantum computing technologies we have not considered here. By doing so, differing system proposals can be compared within a common framework, which gives aspiring quantum engineers a common language for determining the best quantum computing technology for a desired application.

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